A Novel Low Line Regulation CMOS Voltage Reference Without BJTs and Resistors

Changqing Zhang, Xia Wu, Wanling Deng, and Junkai Huang

***Abstract*—A novel CMOS-only low line regulation voltage reference is presented in this paper. An output subcircuit composed of MOSFETs operating in the subthreshold region and saturation region is utilized to eliminate the temperature dependence of mobility and oxide capacitance, and produces a temperature-insensitive voltage reference. No bipolar junction transistors (BJTs) or resistors are used which can decrease the area greatly. By using most of the transistors operating in the subthreshold region, the power dissipation and the supply voltage are reduced. The proposed voltage reference is designed in the standard 0.18 μm CMOS process. The simulation results show that the output voltage is 958.971 mV at TT process corners, a temperature coefficient of 18.6096 ppm/°C range from -20 °C to 110 °C is achieved, the line regulator (LR) of the proposed circuit is 0.037 mV/V from 1.5 V to 2.5 V supply voltage, and the power supply rejection ratio (PSRR) is -75.77 dB at 100 Hz. The active area of the presented voltage reference is 0.0038 mm².**

***Keywords*—voltage reference, resistors, temperature coefficient, LR, PSRR.**

I. Introduction

Voltage reference (VR) circuit is an indispensable unit module in integrated circuit, and is used to provide a stable direct current (DC) reference, which is hardly affected by temperature drift, process variation and voltage fluctuation. Therefore, high precision references with low sensitivity to temperature, process, and supply voltage variations play an important role in many applications, such as analog-to-digital converters (ADC), digital-to-analog converters (DAC), phase-locked loops (PLL), oscillators (OSC), linear voltage regulators, memory and power management chips etc. [1]-[5].

Traditional bandgap reference (BGR) [6]-[8] is implemented by adding two voltages or currents with opposite temperature characteristics, thus producing a voltage independent of absolute temperature. In this method, the base-emitter voltage (V_{BE}) of bipolar junction transistors (BJTs) is usually used to generate a negative temperature coefficient (TC) voltage, and the positive TC voltage is generated by using resistors and thermal voltage (V_T). As V_{EB} is not a linear function of temperature, the voltage with low TC cannot be achieved without first or high order temperature compensation [9]. In order to solve this problem, a large number of compensation circuits are proposed, such as logarithmic-curvature compensation circuit, piecewise liner compensation circuits, etc. [10]-[11]. Although this method can compensate the TC of these circuit well, the use of these BJTs and resistors will occupy a large area, and will also require a high supply voltage and a complex compensation circuit.

Based on such problems, the CMOS VRs without BJTs have been proposed in [12]-[13]. In [12], the mutual temperature compensation principle of the threshold voltage of NMOS and PMOS transistors is utilized to obtain temperature-insensitive VR. In [13], the body bias compensation is employed, and its TC and LR are 48 ppm/°C and 3.4 mV/V respectively. In addition, the voltage reference composed of MOSFETs-only is also proposed in [14]-[15]. In [14], a curvature-compensation method is used to cancel logarithmic temperature dependence of mobility in the circuit, where the TC can be reduced to 7 ppm/°C and the PSRR achieves -43 dB. In [15], the design of VR uses the principle of the theramal compensation of a series composite NMOSTs to obtain reference output voltage whose LR can reach 2.217 mV/V and the TC can be reduced to 19.302 ppm/°C. All of these studies can compensate the TC well, and the BJT or resistor is not introduced in the circuit. However, some new issues such as high LR and low PSRR may follow.

In this paper, we propose a novel CMOS VR. It should be noted that there are no BJTs or resistors used in the circuit. By the use of the transistors operating in the subthreshold region and a MOS resistor operating in the triode region, the area of the proposed VR can be greatly decreased. Since the current source subcircuit uses the feedback technique, the amplifier is omitted, the line regulator (LR) is improved, and the power supply rejection ratio (PSRR) achieves -75.77 dB. The temperature compensation is obtained by using the output subcircuit which is composed of MOSFETs operating in the subthreshold region and saturation region, and it adjusts the output voltage. The proposed design achieves less temperature sensitivity and a smaller line sensitivity. Therefore, the voltage reference can be used in Comparators, A/D and D/A converters, DC-DC converters, and PLLs and so on. The voltage reference can be applied to mini-computers, wearable electronic devices, wireless sensors, smart phones etc. The working principle of this circuit, simulation verification, and other details will be discussed in the following sections.

II. Principle and Architecture of Proposed VR

The principle of our voltage reference is illustrated in Fig. 1.

This work was supported by the Guangdong Natural Science Foundation under Grant 2020A1515010567. C. Zhang, X. Wu, W. Deng, and J. Huang are with the Department of Electronic Engineering, Jinan University, Guangzhou 510630, China. Corresponding author is Junkai Huang (e-mail: hjk196310@126.com), Changqing Zhang (e-mail: 463971191@qq.com), Xia Wu (e-mail: 726558441@qq.com), Wanling Deng (e-mail: dwanl@126.com).

The circuit consists of start-up circuit, current source subcircuit, and output subcircuit. The current source subcircuit uses a MOS resistor MR1 operating in strong-inversion and deep-triode regions instead of ordinary resistors. It generates the current I_{ref}. The output subcircuit accepts current I_{ref} though PMOS current mirrors operating in the saturation region and produces an output voltage (i.e., reference voltage), V_{ref}. All the MOSFETs except for MR1, MN4, MN5, MN7, and PMOS current mirror are operated in the subthreshold region. The circuit generates two voltages with a negative temperature coefficient (TC) and a positive TC. Then, it adds them together to produce a constant voltage with a zero TC. The operation and design considerations of each block will be discussed in the following sections.

A. Principle of temperature compensation

The current source subcircuit is illustrated in the middle of Fig. 1. All the MOSFETs except for MP5 - MP7 and MR1 are operated in the subthreshold region. The subthreshold drain current I_D of a MOSFET is a function of temperature. If the source-drain voltage V_{DS} satisfices $V_{DS} \geq 4V_T$ [16], it can be written as

$$I_D = \mu C_{OX}(\delta - 1)KV_T{}^2 e^{\left(\frac{V_{GS}-V_{TH}}{\delta V_T}\right)} \quad (1)$$

where μ is the temperature-dependent carrier mobility as $\mu(T) = \mu_0(T/T_0)^{-m}$ [17], m is a constant about 1.5-2, C_{OX} is the oxide capacitance per unit area, δ is the subthreshold slope factor, K is the transistor aspect ratio as $K=W/L$, V_T is the thermal voltage and $V_T=K_BT/q$, K_B is the Boltzmann constant, q is the elementary charge, V_{DS} is the drain-source voltage, V_{TH} is the threshold voltage, and V_{GS} is the gate-source voltage.

The structure of negative feedback loop introduced by MP3, MN8, MP5, MP7, MN2 and MN1 is shown in the current source subcircuit of Fig. 1. Due to the negative feedback, the voltage of node c is stable. Therefore gate-source voltage $V_{SG(MP1)}$ in MP1 is equal to the sum of gate-source voltage $V_{SG(MP2)}$ in MP2 and drain-source voltage $V_{DS(MR1)}$ in MR1, i.e.,

$$V_{SG(MP1)} = V_{SG(MP2)} + V_{DS(MR1)} \quad (2)$$

here, $V_{SG(MP1)}$ and $V_{SG(MP2)}$ are the gate-source voltages of MP1 and MP2, respectively. $V_{DS(MR1)}$ is the drain-source voltage of MR1. All symbols in subscript brackets correspond to transistors. Substituting (2) into (3), we can get the expression, i.e.,

$$V_{DS(MR1)} = \delta V_T ln\left(\frac{K_{(MP2)}}{K_{(MP1)}}\right) \quad (3)$$

MOS resistor R_{MR1} are operated in a strong-inversion, deep-triode region, so its resistance R_{MR1} is given by

$$R_{MR1} = \frac{1}{K_{(MR1)}\mu_n C_{OX}(V_{ref}-V_{TH(MR1)})} \quad (4)$$

Using (2), (3), and (4), the bias current I_{ref} of MP7 can be derived as

$$I_{ref} = K_{(MR1)}\mu_n C_{OX}(V_{ref}-V_{TH(MR1)})\delta V_T ln\left(\frac{K_{(MP2)}}{K_{(MP1)}}\right) \quad (5)$$

In the output subcircuit, all the MOSFETs except for MN3 and MN6 are operated in the saturation region, and MN3 and MN6 are operated in the subthreshold region. For I_{ref}, the gate-source voltages of transistors MN3 to MN7 form a closed loop, and the currents of MN4, MN5 are respectively denoted as $3AI_{ref}$ and $2AI_{ref}$, where $A = K_{MP8}/K_{MP7}$. We find that output voltage V_{ref} of the circuit is given by

$$V_{ref} = V_{GS(MN4)} - V_{GS(MN3)} + V_{GS(MN5)} - V_{GS(MN6)} + V_{GS(MN7)} \quad (6)$$

The I-V characteristic of an n-MOSFET operating in the saturation region can be approximated by [18]

$$I_D = \frac{1}{2}\mu C_{OX} K(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (7)$$

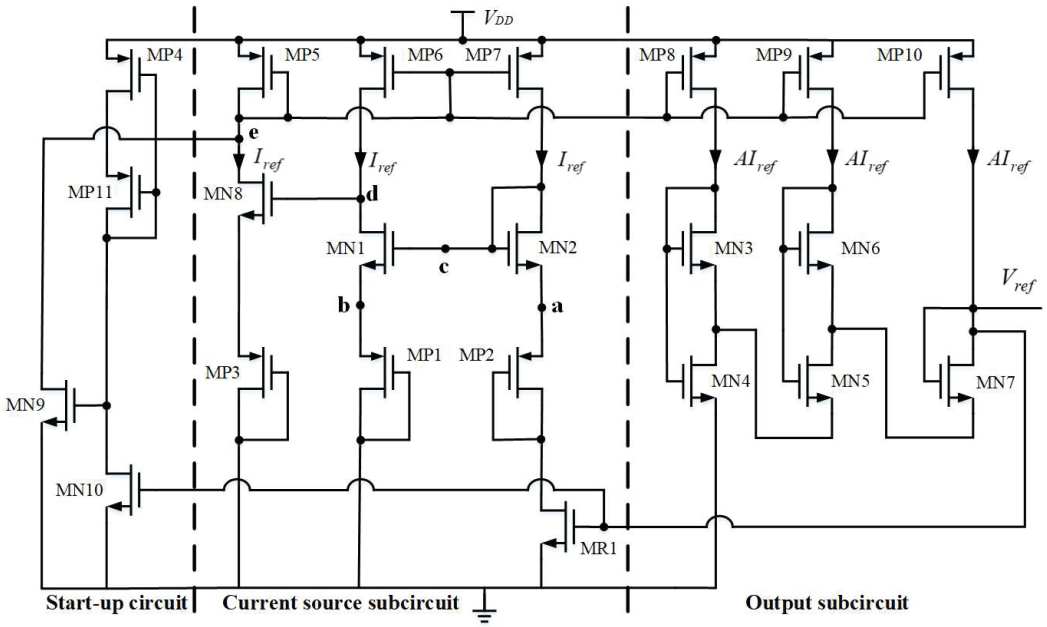

Fig. 1. Schematic of the proposed voltage reference.

where λ is the channel length modulation coefficient. This designed circuit use long channel device to suppress the effect of channel length modulation. Substituting (1), (5) and (7) into (6), the V_{ref} can be rewritten as

$$\begin{aligned} V_{ref} = {} & V_{TH} + \left(\sqrt{\frac{2A}{K_{(MN7)}}} + \sqrt{\frac{4A}{K_{(MN5)}}} + \sqrt{\frac{6A}{K_{(MN4)}}}\right) * \\ & \sqrt{K_{(MR1)}\left(V_{ref} - V_{TH}\right)\delta V_T ln\left(\frac{K_{(MP2)}}{K_{(MP1)}}\right)} - \\ & \delta V_T ln\left(\frac{AK_{(MR1)}\left(V_{GS(MR1)} - V_{TH}\right)\delta ln\left(\frac{K_{(MP2)}}{K_{(MP1)}}\right)}{(\delta-1)K_{(MN\ )}V_T}\right) - \\ & \delta V_T ln\left(\frac{AK_{(MR1)}\left(V_{GS(MR1)} - V_{TH}\right)\delta ln\left(\frac{K_{(MP2)}}{K_{(MP1)}}\right)}{(\delta-1)K_{(MN3)}V_T}\right) \end{aligned} \tag{8}$$

where we assumed that the mismatch between the threshold voltages of the transistors can be ignored. Besides, the temperature dependence of the threshold voltage can be given by

$$V_{TH} = V_{TH0} - \alpha T \tag{9}$$

where V_{TH0} is the threshold voltage at 0 K, α is TC of V_{TH} [11]. Substituting (9) into (8), the V_{ref} can be given by

$$\begin{aligned} V_{ref} = {} & \left(\sqrt{\frac{2A}{K_{(MN7)}}} + \sqrt{\frac{4A}{K_{(MN5)}}} + \sqrt{\frac{6A}{K_{(MN4)}}}\right) * \\ & \sqrt{K_{(MR1)}\left(V_{ref} - V_{TH\ } + \alpha T\right)\delta V_T ln\left(\frac{K_{(MP\ )}}{K_{(MP1)}}\right)} \\ & -2\delta V_T ln\left(\frac{AK_{(MR1)}\left(V_{ref} - V_{TH0} + \alpha T\right)\delta ln\left(\frac{K_{(MP\ )}}{K_{(MP\ )}}\right)}{(\delta-1)V_T}\right) \\ & +\delta V_T ln\left(K_{(MN6)}K_{(MN3)}\right) + V_{TH0} - \alpha T \end{aligned} \tag{10}$$

In this designed circuit, when the TC has the smallest value, the relation of $V_{ref} - V_{TH0} \ll KT$ can be developed [19]. As a result, V_{ref} can be rewritten as

$$\begin{aligned} V_{ref} = {} & V_{TH0} + \left(\frac{\delta K_B ln\left(K_{(MN6)}K_{(MN3)}\right)}{q} + B - \alpha\right)T - \\ & \frac{2\delta K_B}{q} ln\left(\frac{AK_{(MR\ )}q\delta\alpha ln\left(\frac{K_{(MP\ )}}{K_{(MP1)}}\right)}{(\delta-1)K_B}\right)T \end{aligned} \tag{11}$$

where

$$\begin{aligned} B = {} & \left(\sqrt{\frac{2A}{K_{(MN\ )}}} + \sqrt{\frac{4A}{K_{(MN\ )}}} + \sqrt{\frac{6A}{K_{(MN4)}}}\right) * \\ & \sqrt{\frac{K_{(MR\ )}\alpha\delta K_B ln\left(\frac{K_{(MP\ )}}{K_{(MP1)}}\right)}{q}}. \end{aligned}$$

According to (11), a zero TC voltage can be obtained by choosing a proper $k_{(i)}$ on condition that

$$\begin{aligned} & \frac{\delta K_B ln\left(K_{(MN6)}K_{(MN3)}\right)}{q} + B - \alpha - \\ & \frac{2\delta K_B}{q} ln\left(\frac{AK_{(MR1)}q\delta\alpha ln\left(\frac{K_{(MP\ )}}{K_{(MP1)}}\right)}{(\delta-1)K_B}\right) = 0 \end{aligned} \tag{12}$$

Therefore, we can get a high-precision voltage reference based on the above temperature compensation principle.

B. Negative feedback analysis

The channel length modulation effect causes variation of the output voltage and the bias current when the supply voltage varies [20]. The LR performance is a DC parameter, which represents the variation of output voltage caused by the input supply change. On the other hand, PSRR is defined as $PSRR = 20lg\left(\Delta V_{ref}/\Delta V_{DD}\right)$. It is not only the complement of supply gain but it also includes the entire frequency spectrum. Therefore, A voltage reference that is insensitive to the supply voltage is very important. In Fig. 1, a negative feedback loop composed of MP3, MN8, MP5, MP7, MN2 and MN1 is introduced to improve the performances of PSRR and LR. If the voltage V_d of the node d rises with the supply voltage variation, V_e would drop, and V_c would rise. Since the gain of the negative feedback loop is greater than the positive feedback loop gain introduced by MN1, MN8, MP5 and MP6, V_d would fall at last. In addition, MP1-MP3 working in the subthreshold region are diode connected, and their V_{DS} voltages are much larger than $4V_T$, so they are almost constant for the small variation of bias current. Fig. 2 shows the small signal model of the current source subcircuit at low frequencies.

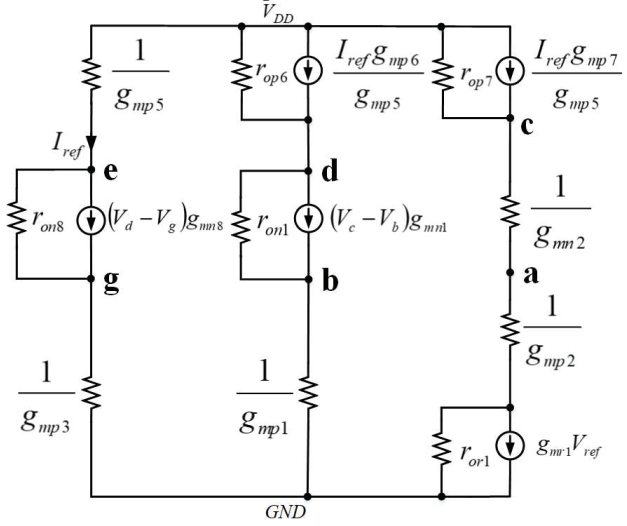

Fig. 2. Small-signal model of the current source subcircuit.

$$I_{ref} = (V_{DD} - V_e)g_{mp5} \tag{13}$$

$$I_{ref} = \frac{V_e - V_g}{r_{on8}} + (V_d - V_g)g_{mn8} = V_g g_{mp3} \tag{14}$$

$$\begin{aligned} (V_{DD} - V_e)g_{mp6} + \frac{V_{DD} - V_d}{r_{op6}} = {} & \frac{V_d - V_b}{r_{on1}} + (V_c - V_b)g_{mn1} \\ & = V_b g_{mp1} \end{aligned} \tag{15}$$

$$(V_{DD} - V_e)g_{mp7} + \frac{(V_{DD} - V_c)}{r_{op7}} = (V_c - V_a)g_{mn2} \tag{16}$$

$$\begin{aligned} V_a = {} & \left[(V_c - V_a)g_{mn2} - V_{ref}g_{mr1}\right]r_{or1} \\ & +(V_c - V_a)\frac{g_{mn2}}{g_{mp2}} \end{aligned} \tag{17}$$

Herein, g_{mni} and g_{mpi} represent the transconductances of MNi and MPi, respectively. The output resistances of MPi and MNi are marked as r_{opi} and r_{oni}, respectively. V_{DD} is the supply voltage. Through (13)-(17), we can get the expression. i.e.,

$$V_{ref} = \frac{V_g}{g_{mr1}}\left(\frac{g_{mp3}\,g_{mp7}}{g_{mp5}} - \frac{A}{r_{op7}}\right) + \frac{V_{DD}}{g_{mr1}r_{op7}} \tag{18}$$

where

$$A = \frac{g_{mn1}+g_{mp1}}{g_{mp1}g_{mn1}}\left(\frac{g_{mp3}g_{mp6}}{g_{mp5}} - \frac{g_{mp3}+g_{mn8}}{g_{mn8}r_{op6}}\right) - \frac{g_{mn8}+g_{mp3}}{r_{on1}g_{mn8}g_{mn1}}$$

Fig. 3 shows the small signal model of the output subcircuit. Similarly, we can get the following expressions:

$$\frac{V_{DD}-V_f}{r_{op8}} + (V_{DD}-V_e)g_{mp8} = (V_f - V_h)g_{mn3} \quad (19)$$

$$\frac{V_{DD}-V_w}{r_{op9}} + (V_{DD}-V_e)g_{mp9} = (V_w - V_i)g_{mn6} \quad (20)$$

$$\frac{V_{DD}-V_{ref}}{r_{op10}} + (V_{DD}-V_e)g_{mp10} = (V_{ref} - V_i)g_{mn7} \quad (21)$$

$$(V_w - V_i)g_{mn6} + (V_{ref} - V_i)g_{mn7} = \frac{V_i - V_h}{r_{on5}} + (V_w - V_h)g_{mn5} \quad (22)$$

$$(V_f - V_h)g_{mn3} + (V_w - V_i)g_{mn6} + (V_{ref} - V_i)g_{mn7} = \frac{V_h}{r_{on4}} + V_f g_{mn4} \quad (23)$$

Through (19)-(23), we can get

$$V_{ref} = V_g\left(\frac{g_{mp3}g_{mp10}}{g_{mn7}g_{mp5}} + \frac{\frac{g_{mp3}}{g_{mp5}g_{mn4}}B+D}{\frac{g_{mn6}}{g_{mn5}}+g_{mn5}-g_{mn6}}\right) + V_{DD} * \left(\frac{1}{g_{mn7}r_{op10}} + \frac{C}{g_{mn4}} - \frac{1}{g_{mn5}r_{op10}} - \frac{g_{mn6}-g_{mn5}}{g_{mn6}r_{op9}}\right) \quad (24)$$

where

$$B = g_{mp8} + g_{mp9} + g_{mp10} - \frac{g_{mn4}g_{mp8}}{g_{mn3}}$$

$$C = \frac{1}{r_{op8}} + \frac{1}{r_{op9}} + \frac{1}{r_{op10}} - \frac{g_{mn4}}{g_{mn3}r_{op8}}$$

$$D = \frac{g_{mp3}g_{mp10}}{g_{mn5}g_{mp5}} + \frac{g_{mp3}g_{mp9}(g_{mn6}-g_{mn5})}{g_{mn6}g_{mp5}}$$

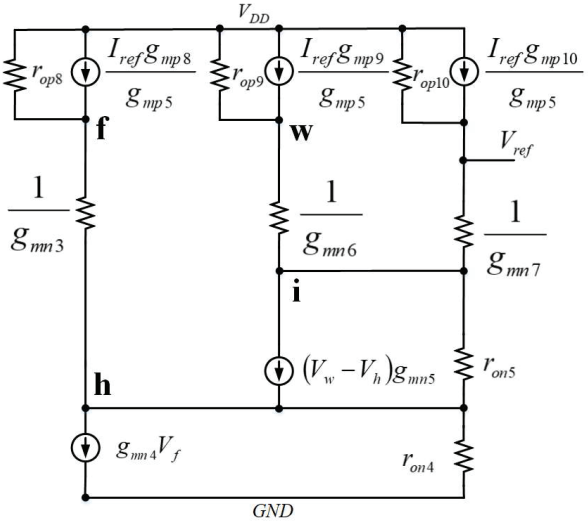

Fig. 3. Small-signal outputt subcircuit.

Using (18) and (24), V_{ref}/V_{DD} can be written as

$$\frac{V_{ref}}{V_{DD}} = \frac{E - \left(\frac{g_{mp3}g_{mp7}r_{op7}}{g_{mp5}} - A\right)F}{\frac{g_{mp3}g_{mp7}r_{op7}}{g_{mp5}} - A - g_{mr1}r_{op7}E} \quad (25)$$

where

$$E = \left(\frac{g_{mp3}g_{mp10}}{g_{mn7}g_{mp5}} + \frac{\frac{g_{mp3}}{g_{mp5}g_{mn4}}B+D}{\frac{g_{mn6}}{g_{mn5}}+g_{mn5}-g_{mn6}}\right)$$

$$F = \frac{1}{g_{mn7}r_{op10}} + \frac{C}{g_{mn4}} - \frac{1}{g_{mn5}r_{op10}} - \frac{g_{mn6}-g_{mn5}}{g_{mn6}r_{op9}}$$

From (25), we can deduce that the sensitivity of V_{ref} to V_{DD} is proportional to g_{mp3}/g_{mp5}, g_{mr1}, and g_{mp8}. By adjusting the transistor aspect ratio of MP9, MN5, MN6, etc., the LR can be further improved. Therefore, the VR independent of V_{DD} can be obtained by reasonably adjusting the aspect ratio of MPi and MNi.

III. Simulation Results and Discussion

In order to verify the performance of the proposed VR, a series of simulation results have been implemented under the TSMC 0.18 μm CMOS process.

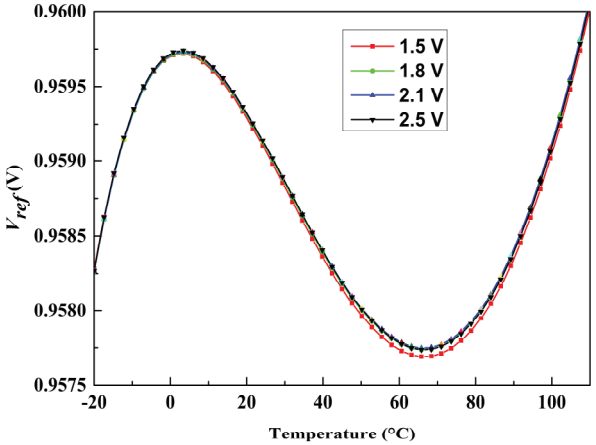

Fig. 4. V_{ref} versus temperature at different supply voltages.

Fig. 4 shows the simulation results of the output voltage V_{ref} versus temperature at various supply voltages. When the supply voltage varies from 1.5 V to 2.5 V, the minimum and maximum values of V_{ref} in the range from -20 to 110 ºC are 958.971 mV and 959.008 mV, respectively. Under four different supplied voltages, the average value of TC is about 18.6893 ppm/°C, and the maximum deviation of the temperature coefficient is 0.1598 ppm/°C.

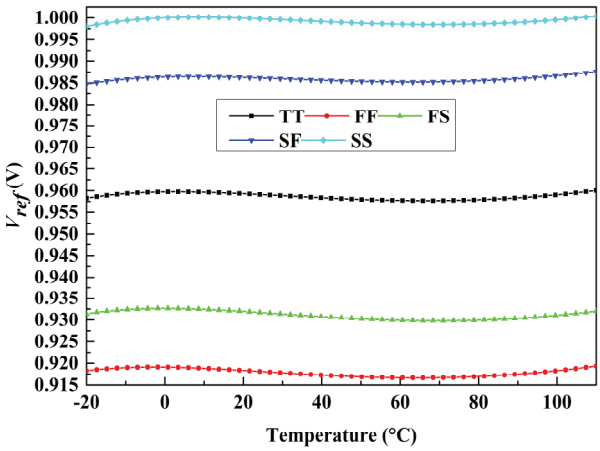

Fig. 5. V_{ref} versus temperature at different process corners.

The V_{ref} of the proposed circuit versus temperature at

different process corners is shown in Fig. 5, where the best case occurs at the SS process corner whose TC is 18.2362 ppm/°C, while the worst case occurs at the FS process corner whose TC is 23.3690 ppm/°C, and the difference between them is 5.1328 ppm/°C. This simulation result is consistent with the derivations of (10) to (12). Therefore, under different supply voltages and process corners, the output voltage V_{ref} has a stable TC.

Fig. 6 shows that V_{ref} varies with V_{DD} at different temperatures. Obviously, curves with different temperatures have similar trends and due to the proposed circuit structure, the circuit begins to output the stable V_{ref} after V_{DD} = 1.5 V.

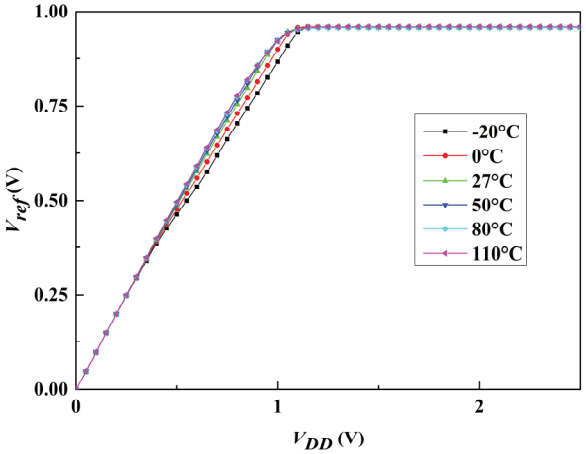

Fig. 6. V_{ref} versus V_{DD} at different temperatures.

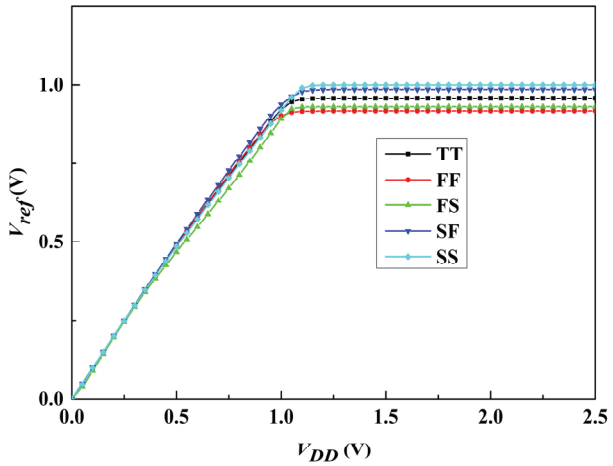

Fig. 7. V_{ref} versus V_{DD} at different process corners.

Fig. 7 shows that V_{ref} varies with V_{DD} at different process corners when the supply voltage is 1.5 V. It is clearly that the output voltage is almost constant when the supply voltage is greater than 1.5 V, and all the transistors work in their corresponding regions. Under the TT corner, when the supply voltage sweeping from 1.5 V to 2.5 V, V_{ref} changes from 959.971 mV to 959.008 mV. Consequently, the LR can be calculated to be 0.037 mV/V. The best and worst LR are 0.025 mV/V and 0.053 mV/V in FS and SF corners, respectively. Thence, it can be seen that this output voltage is not affected by power supply voltage and temperature changes. This result is consistent with the derivation of (25). The low LR can be achieved due to the negative feedback structure, which improves the performance of the proposed circuit.

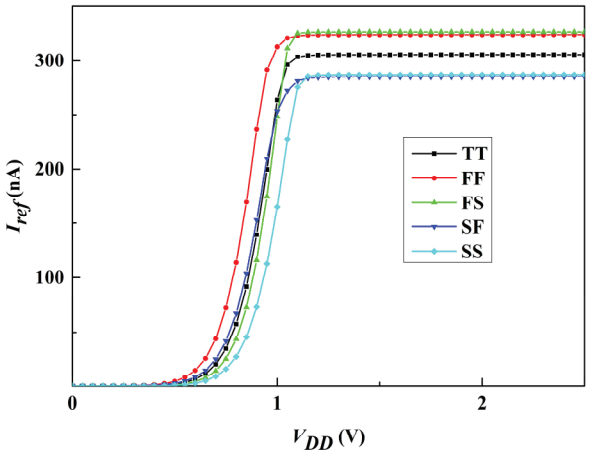

Fig. 8. I_{ref} versus V_{DD} at different process corners.

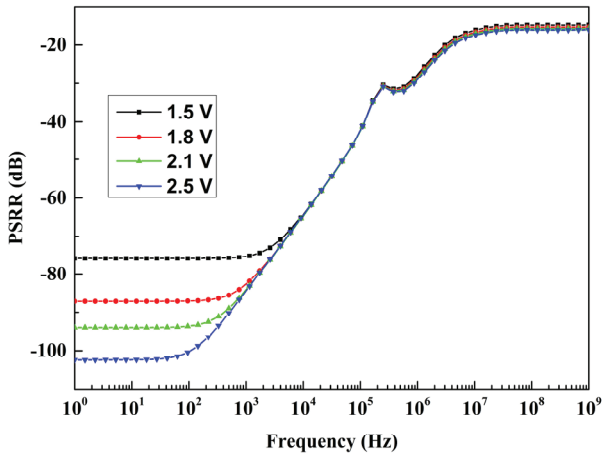

Fig. 9. PSRR versus frequency at different power supplies.

TABLE I
SUMMARY OF CRITICAL PARAMETERS AT FIVE KINDS OF PROCESS CORNERS.

corners		TT	FF	FS	SF	SS
TC (ppm/°C) @ V_{DD}=1.5 V		18.6096	22.5417	23.3690	22.3891	18.2362
PSRR (dB)	100 Hz V_{DD}=1.5 V	-75.77	-75.08	-88.69	-70.46	-79.18
LR (mV/V)		0.037	0.037	0.025	0.053	0.031
V_{ref} (mV) @ V_{DD}=1.5 V		958.971	917.955	931.540	986.055	999.698

The simulation curve of the bias current I_{ref} versus V_{DD} at different process corners is presented in Fig. 8. It is worth noting that for all the process corners, the supply current is almost constant in the range from 1.5 V to 2.5 V. Under TT corner, the offset of this current I_{ref} is only 60 pA when the supply voltage changes 1.5 V, and the minimum and maximum deviation values of I_{ref} in the five corners are 52 pA and 70 pA, respectively. The current is almost independent of the supply voltage. Moreover, when the power supply voltage is 1.5 V, the total current consumed by this circuit at the TT corner is 3.77 µA.

Fig. 9 shows that PSRR varies with frequency at four different V_{DD} cases. From the picture, when V_{DD} is 2.5 V, the PSRR achieves -100.3 dB at 100 Hz. Under the condition of V_{DD} = 1.5 V, the PSRR of the proposed VR is around -75.77 dB at 100 Hz.

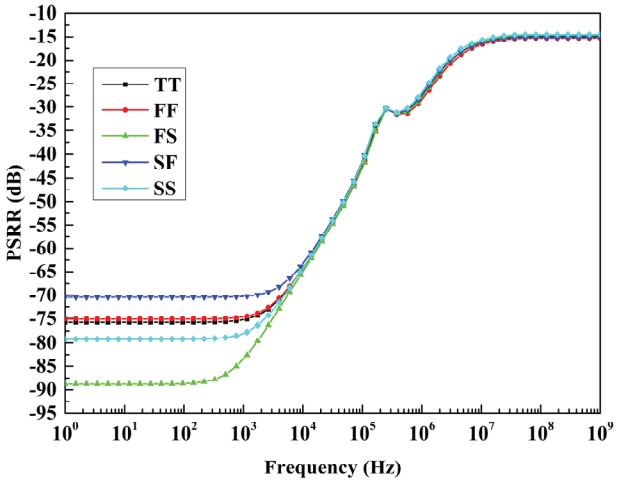

Fig. 10. PSRR versus frequency at different process corners.

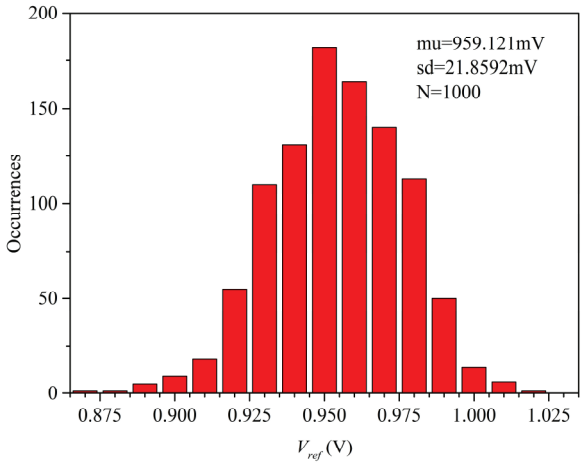

Fig. 11. Monte-Carlo simulation result of V_{ref}.

Fig. 10 illustrates the simulation curves of PSRR versus frequency at different process corners when the supply voltage is 1.5 V. When the frequency is 100 Hz, the best and worst PSRR are -88.69 dB and -70.46 dB in FS and SF corners, respectively. Through the negative feedback technique, the variation of I_{ref} is very small (see Fig. 8), the PSRR performance also benefits from this negative feedback structure.

The sensitivity of the output reference voltage is evaluated by Monte Carlo simulation 1000 runs, which takes into account the effects of the mismatch and process variations in all the transistors of the proposed reference. When V_{DD} is 1.5 V, Monte-Carlo simulation result of V_{ref} at 27 °C is shown in Fig. 11. It can be clearly observed that the average value of V_{ref} is 959.121 mV, the standard deviation is 21.8592 mV, and the coefficient of variation σ/µ is about 2.27%.

From (12), we can see that TC of the proposed reference can become smaller by increasing $K_{(MN3)}$ and $K_{(MN6)}$ or decreasing $K_{(MN4)}$, $K_{(MN5)}$ and $K_{(MN7)}$. Besides, the PMOS current mirror uses the same large size transistors to reduce current mismatch and channel length modulation effects. As shown in Fig. 12, the PMOS current mirror occupies a large area in the layout. However, the VR circuit proposed in this paper is simple in structure and without using resistors and BJTs. Therefore, the final total layout area is only 0.0038 mm^2 (66 µm ∗ 58 µm).

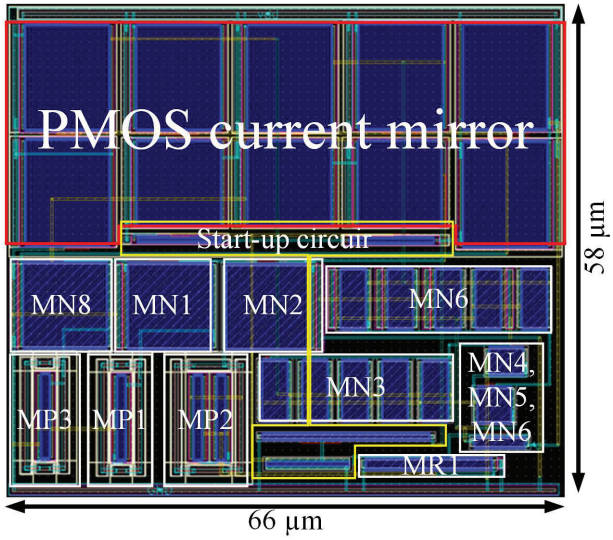

Fig. 12. Layout of the proposed VR.

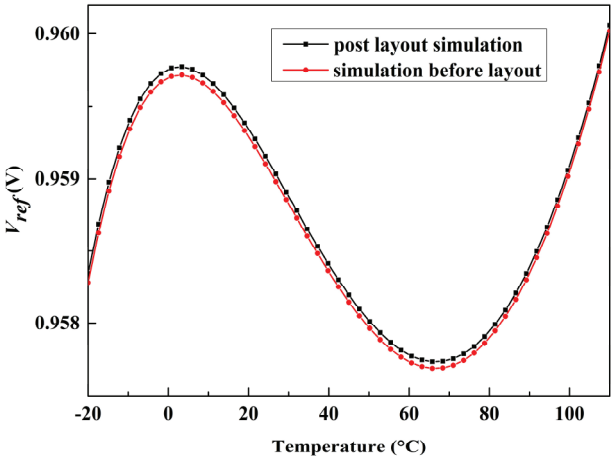

Fig.13. Comparison between simulation and post layout simulation at TT corner.

The comparison of output voltage V_{ref} as a function of temperature between simulation and post layout simulation is shown Fig. 13. From the picture, we can know that the results

TABLE II
COMPARISONS AMONG THE PROPOSED CIRCUIT AND OTHER VOLTAGE REFERENCE CIRCUITS.

Parameter	This work	[11]	[12]	[13]	[14]	[15]
Process (μm)	0.18	0.18	0.35	0.13	0.065	0.18
BJTs	None	None	None	None	None	None
Resistors	None	Yes	Yes	None	None	None
Temperature range (˚C)	-20-110	-20-80	0-130	0-100	-40-125	-40-85
Supply voltage (V)	1.5-2.5	1.35-1.8	1.8/3/4.5	1.2-2.3	1.2-2.0	1.25-2.0
V_{ref} (mV)	958.971	630	847.5	781	594.5	536.01
TC (ppm/˚C)	18.6096	14.1	13.6/11.8/12.7	48	7	19.302
LR (mV/V)	0.037	0.298	0.185	2.6554	0.076	2.217
PSRR (dB)	-75.77	-75.7	-72	-51.4	-43	-51.4@10 Hz
@100Hz	@1.5 V	@1.6 V	@3.0 V	@1.2 V	@ 1.2 V	N/A
Area (mm^2)	0.0038	0.015	0.014	0.014	0.03	0.0077

of the simulation and post layout simulation only have a maximum difference of 0.054 mV, Therefore, the design of the circuit is reasonable.

The critical technical performances of the proposed voltage reference at five different process corners are shown in details in Table I. Under these five process corners, the worst TC, PSRR, LR are 23.3690 ppm/°C, -70.46 dB, 0.053 mV/V respectively. In addition, the maximum deviation of each performance is also very small. Therefore, the proposed circuit meets the design requirements. The characteristics of proposed circuit compared to other voltage reference circuits are shown in Table II where TC and PSRR of the proposed circuit are optimized, and the LR and area are significantly improved.

IV. CONCLUSION

This paper proposes a novel low LR CMOS voltage reference without BJTs and resistors, which is area efficient and less sensitive to temperature. The design is achieved by the TSMC 0.18 μm CMOS process. The output voltage with a low TC is obtained by utilizing output subcircuit composed of MOSFETs operating in the subthreshold region and saturation region. Through the use of the negative feedback technology, the amplifer is omitted, and the low LR can be realized. In the range of -20 to 110 ºC, the proposed VR achieves TC of 18.6096 ppm/ºC for a 1.5 V supply, while the PSRR is -75.77 dB at 100 Hz. The maximum variation of output voltage is only 0.037 mV from 1.5 V to 2.5 V supply voltage. The proposed VR with low TC, low LR, and high PSRR, can be attractive in high-precision systems.

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Changqing Zhang received the B.A. degree from Hunan University of Science and Engineering, YongZhou, China, in 2017. He is currently pursuing the M.S. degree with Jinan University, Guangzhou, China. His current research interest includes the design of integrated circuit and system on chip.

Wanling Deng received the B.S. and Ph.D. degrees in electrical engineering from the South China University of Technology, Guangzhou, China, in 2003 and 2008, respectively. Since 2008, she has been an Associate Professor with the Department of Electronic Engineering, Jinan University, Guangzhou. Her current research interests include thin-film transistor (TFT) devices and physics, particularly poly-Si TFT and AOS TFT modeling.

Xia Wu received received the B.S. degree in electrical engineering from Jinan University, Guangzhou, China, in 1997 and the M.S. degree in education management from South China Normal University, Guangzhou, China, in 2009 respectively. Since 1997, she has worked in Jinan University. Her current research interests include semiconductor device physics and test methods.

Junkai Huang received the B.S. degree in applied physics and the M.S. degree in semiconductor device from Jinan University, Guangzhou, China, in 1985 and 1990, respectively, and the Ph.D. degree from the Institute of Microelectronics, South China University of Technology, Guangzhou, in 2011. He is currently a Professor with Jinan University. His current research interests include thin-film transistors' modeling, simulation, and integrated circuit design.